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Lab & Production Materials

User protocol for graphene FET GRFETS20

Basic handling instructions

The graphene used in our GFETs is high-quality monolayer CVD graphene and highly prone to damage by external factors. To maintain the quality of your devices, we recommend taking the following precautions:

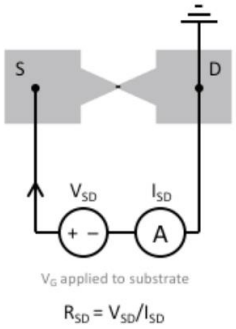
- Be careful when handling the GFET chip that tweezers do not make contact with the device area. Metallic tweezers should be avoided, as they can damage/scratch the chip edges/surface
- Treat the devices as sensitive electronic devices and take precautions against electrostatic discharge
- Ideally store in inert atmosphere or under vacuum in order to minimize adsorption of unknown species from the ambient air
- Do not ultrasonicate the GFET dies
- Do not apply any plasma treatment to the GFET dies
- Do not subject the GFET dies to strongly oxidizing reagents

Testing protocol:

2-probe devices

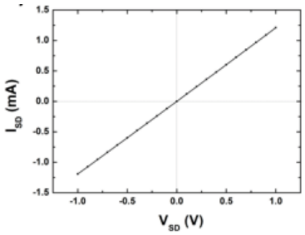
These devices allow field-effect measurements by simultaneously applying two voltages:

- Source-drain voltage (V_{SD}): applied between the two probes (source and drain), while one of them is grounded (see Figure below).



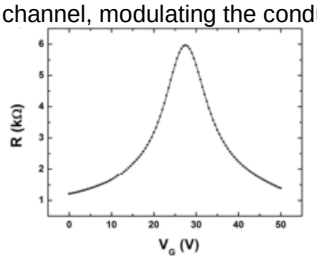
Scheme of the 2-probe device, with the corresponding electrical measurement configuration.

V_{SD} enables the transport of charge carriers through the graphene channel, with an associated source-drain current (I_{SD}). V_{SD} can be varied in order to get the desired I_{SD} outcome (see Figure below).



Typical output curve measured at room temperature in vacuum.

• Gate voltage (V_G): applied to the Si on the substrate. V_G creates an electric field on the graphene channel, modulating the conductivity of graphene (see Figure below).



Typical transfer curve measured at V_{SD}= 20mV (right), measured at room temperature in vacuum.

The Si can be contacted either from the top surface by scratching the 90 nm-thick SiO_2 with a diamond pen in one of the chip corners; or alternatively from the underside of the chip, for instance using a probe station chuck.

The resistivity of graphene is usually expressed per thickness unit, i.e. the so-called sheet resistance: $R_S = R_{SD}\frac{W}{L1}$, wherein W and L1 are the width and inner length of the graphene channel, respectively. The field-effect mobility (μ_{FE}) can be calculated by using the following equation:

$$\mu_{FE} = g \cdot \frac{1}{C_{SiO2}},$$

where:
• g = dσ/dV_G is the transconductance, being σ=1/R_S,
• CSiO2 is the capacitance per unit area of the 90 nm-thick SiO2 dielectric.
μ_{FE} is usually calculated using the maximum transconductance. Note that this calculation includes the voltage drop at the graphene/metal interface, therefore μ_{FE} is a lower bond of the intrinsic mobility of the graphene channel.

The field-effect charge carrier density (n_{FE}) is calculated as follows: $n_{FE} = \mu_{FE} \cdot R_S/e$
In order to extract the residual carrier concentration n_0, i.e. the charge carrier density at the Dirac point, we can use the following expression: $n_{FE} = \sqrt{n_0^2 + n_G^2},$
where n_G is the gate-induced charge carrier density, which is calculated from the following equation:

$$V_G - V_D = \frac{e}{C_{SiO2}} n_G + \frac{\hbar v_F \sqrt{\pi \cdot n_G}}{e},$$

where V_D is the Dirac voltage and ν_F is the Fermi velocity.

Doping-reduction treatment

Graphene on SiO_2 is often p-doped after exposure to air due to the adsorption of water molecules and other adsorbates with the effect that the Dirac point is shifted to positive gate voltages and can cause the Dirac voltage to be located out of the recommended gate voltage range. In addition, a large hysteresis is observed between the forward and backward sweeps of a transfer curve.
Immersing the graphene FET chip in acetone for at least 12h reduces doping. After that, the chip should be immediately rinsed with IPA, properly dried with an Ar or N_2 gun, and shortly introduced into the measurement equipment. In order to preserve the effectivity of this treatment, electrical characterization should be carried out in inert atmosphere or vacuum.
In addition, storage of the chips in a low humidity environment (N_2 cabinet, desiccator, or vacuum) is highly recommended.